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Charissa Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Chang Hun HAN**, a citizen of the Republic of Korea, residing at #101-605 Hyundai 1-cha Apt., Changjeon-dong, Icheon-si, Gyeonggi-do 467-731, Korea have invented new and useful **METHODS FOR FABRICATING NON-VOLATILE MEMORY DEVICES**, of which the following is a specification.

METHODS FOR FABRICATING NONVOLATILE MEMORY DEVICES

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to methods for fabricating nonvolatile memory devices and, more particularly, to methods for fabricating a multi-bit flash memory cell by forming two (2) floating gates in one cell without increasing the cell size.

BACKGROUND

[0002] In a one-bit type EEPROM (electrically erasable programmable read only memory) cell, a device isolation layer 13 defining an active region and a device isolation region is formed in a substrate. A tunnel oxide 15 and a floating gate 17 are layered in the active region. In other words, the one-bit cell includes one floating gate per cell. The device isolation layer is formed through a LOCOS (local oxidation of silicon) or an STI (shallow trench isolation) process.

[0003] On the other hand, a two-bit type cell comprises two floating gates per cell. Fig. 1 is a cross-sectional view of a conventional EEPROM cell of the two-bit type. The two-bit type of EEPROM cell can share two (2) floating gates in one cell, whereas the one-bit type of EEPROM cell includes one floating gate in one cell.

[0004] However, in the prior art, when two floating gates have been formed in one cell, the cell size has increased as large as the lithographic minimum feature size (hereinafter referred to as "F"), such as a space size

between the two floating gates. The minimum size of "F" is irrelevant to the smooth operation of a cell. Rather it is necessarily caused by limitations of the mask patterning. Therefore, it is preferable to reduce the "F" value in order to decrease cell size.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Fig. 1 is a cross-sectional view of a conventional 2-bit type EEPROM cell.

[0006] Figs. 2a through 2g are cross-sectional views illustrating an example process for fabricating a nonvolatile memory device in accordance with the teachings of the present disclosure.

DETAILED DESCRIPTION

[0007] Referring to the example of Fig. 2a, a trench isolation layer 33 is formed in a silicon substrate 31. The trench isolation layer 33 defines an active region and a device isolation region in the substrate 11. An oxide layer 35 (for the formation of a tunnel oxide) and a polysilicon layer 37 (for the formation of a floating gate) are then sequentially formed on the substrate 31 and the trench isolation layer 33.

[0008] Referring to Fig. 2b, a first sacrificial layer 39 is formed on the polysilicon layer 37. The first sacrificial layer 39 is preferably formed of one selected from the group consisting of TEOS (tetraethyl orthosilicate) oxides and nitride.

[0009] Referring to Fig. 2c, a photoresist pattern 41 is formed on the first sacrificial layer 39. The width of a region to be etched through the photoresist pattern 41 is the lithographic minimum feature size (F).

[0010] Referring to Fig. 2d, an etching process is performed using the photoresist pattern 41 as a mask to remove some part(s) of the first sacrificial layer 39 until the polysilicon layer 37 is exposed through the photoresist pattern 41. At the same time, polymers generated from the etching of the first sacrificial layer 39 are attached to the sidewalls of the etched first sacrificial layer 39 to form polymer layers 43. The polymer layers 43 are used as a second sacrificial layer. Here, the polymer layers 43 are formed so that the space between the adjacent polymer layers 43 is preferably between 300□ and 1200□.

[0011] Referring to Fig. 2e, the exposed portion(s) of the polysilicon layer 37 and the oxide layer 35 beneath those portion(s) are etched by a dry etching process using the polymer layers 43 and the photoresist pattern 41 as a mask until the surface of the substrate 31 is exposed.

[0012] Referring to Fig. 2f, the polymer layers 43, the first sacrificial layer 39, and the photoresist pattern 41 are removed. As a result, a floating gate 37a and a tunnel oxide 35a are formed on the substrate 31. The width of the floating gate 37a is, thus, increased by the widths of the adjacent two polymer layers 43 attached to the sidewalls of the etched first sacrificial layer. As a result, the coupling ratio increases.

[0013] Referring to Fig. 2g, an insulating layer 45 and a polysilicon layer 47 (to form a control gate) are deposited over the substrate and the floating gate 37a and the tunnel oxide 35a.

[0014] The example methods disclosed herein can increase the width of a floating gate by using polymer layers 43 in fabricating a two-bit type memory cell. The increased width ensures a higher coupling ratio as compared to the coupling ratio of a conventional two-bit type cell. The example methods disclosed herein can reduce cell size and improve device reliability by reducing internal voltage.

[0015] From the foregoing, persons of ordinary skill in the art will appreciate that the above disclosed methods for fabricating nonvolatile memory devices can reduce the space between floating gates by forming polymer spacers. This reduction of the space between the gates increases the length of the floating gates without increasing the cell size.

[0016] An example method disclosed herein comprises: forming a trench isolation layer defining an active region and a non-active region in a substrate; forming an oxide layer for the formation of a tunnel oxide and a polysilicon layer for formation of a floating gate; forming a sacrificial layer on the polysilicon layer; forming a photoresist pattern on the sacrificial layer; performing an etching process using the photoresist pattern as a mask to remove some part of the sacrificial layer until the polysilicon layer is exposed through the photoresist pattern; and, at the same time, attaching polymers on the sidewalls of the etched sacrificial layer to form polymer layers, the polymers being generated from the etching of the sacrificial layer; and

forming a floating gate and a tunnel oxide by removing some part of the polysilicon layer and the oxide layer using the polymer layers and the photoresist pattern as a mask.

[0017] Although certain example methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. On the contrary, this patent covers all methods, apparatus and articles of manufacture fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.